USER MANUAL

HVS/UM9802
I^2C-bus Register Specification for the SAA 4977 V1C

Philips
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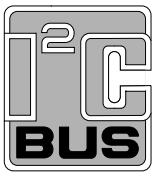
REVISION HISTORY

Version	Remarks
0.1	DRAFT; 14.08.96
0.2	Update I²C REGs 24,25; 20.08.96
0.3	Update REG7: ENA_HWE_ROUGH; 21.08.96
1.0	First Release; refers to BESIC-SW from V0.34 until V1.0; 31.10.96 (This UM describes the I²C interface of the BESIC for a single memory concept or a PROZONIC concept. The µC ROM of the first BESIC samples contain this interface. MELZONIC control (SAA4991) is not possible via the I²C interface described in this document)
2.0	Second Release; refers to BESIC-SW starting with V2.0; 28.02.97 This document describes a new I²C interface of the BESIC including the MELZONIC control in addition to the features described in the first release document. An external µC ROM of the first BESIC samples will contain this new I²C interface. A new BESIC version, which will be developed, contains the new interface.
2.1	HVS/UM9704, 12.12.97, update of UM9701 V2.0
1.0	HVS/UM9802, 06.02.98 This user manual refers to the final BESIC version SAA 4977 V1C. This software sup-



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Report No.: HVS/UM9802

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Preface

The user manual describes the I^2C-bus register interface of an IPQ slave microcontroller (80C51 core), which is a part of the BESIC (SAA 4977). The described interface refers to the BESIC version V1C (see Revision History).

The BESIC is a videoprocessing IC providing analog interfacing, video enhancing features, memory controlling and the embedded 80C51 microprocessor core. The internal (slave) microcontroller is used as an interpreter between a main (master) µC and the Datapath Control in BESIC. It controls the embedded memory controller as well. In case of a two field memory concept either the PROZONIC (SAA4990; external) or MELZONIC (SAA4991; external) is supported by the software. In the single field concept the LIMERIC (SAA 4945) can be controlled via the SAA 4977 as well.

The software of the SAA 4977 V1C is written according to the Software Creation Process [9].

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1. Introduction

The UM9705 V1.0 describes the I^2C interface of the SAA 4977 V1C. The software of this BESIC version supports all the concepts described in the application notes AN97057 and AN 97071. This means it supports the single field concept, the PROZONIC concept and the MELZONIC concept.

1.1 Definitions, Acronyms and Abbreviations

AFF	Acquisition field frequency
BESIC	SAA4977 V1C
HEX	Hexadecimal
HOST interface	BESIC Interface towards 8051 microprocessor core
IIC	Inter Integrated Circuit
IPQCS	Improved Picture Quality Control Software
IPQ µC	Improved Picture Quality slave microcontroller
LFR	Line Flicker Reduction by median filtering
LIMERIC	Line memory and Noise Reduction IC
MELZONIC	Motion Estimation/compensation, Line flicker reduction, ZOom and Noise reduction IC
MPD	Movie Phase Detection
MPIP	Multi picture in picture with external PIP processor
NR	Noise reduction (adaptive)
PROZONIC	PROgressive Scan, Zoom and Noise reduction IC
SCP	Software Creation Process
VDFL	Vertical Deflection pulse (output of memory controller)

1.2 References

[1] Philips Semiconductors Software Creation Process V1.0; Wilko van Asseldonk, Marc de Smet; April 9th, 1996

[2] Tentative Device Specification for BESIC; 06.08.96; A. Kannengiesser

[3] Tentative Device Specification Control Part BESIC; 24.06.96; G. Stäcker, H. Waterholter

[4] 80C51 microcontroller order form

[5] 80C51 microcontroller Core Specification V1.2; 22.02.96; P. Klapproth

[6] Datapath Control Register; 13.08.96; A. Kannengiesser

[7] Application Note, MK8 Module, AN97057; H. Waterholter

[8] Application Note, MK9 Module, AN97071; H. Waterholter

[9] Software Creation Process, Nov. 18th 1997

2. General

The IPQ µC receives register bytes via the I^2C-bus from the master µC and sends itself 1 status byte plus following read registers whenever addressed with R/W = 1. The I^2C register bytes received are written into RAM of the IPQ µC.

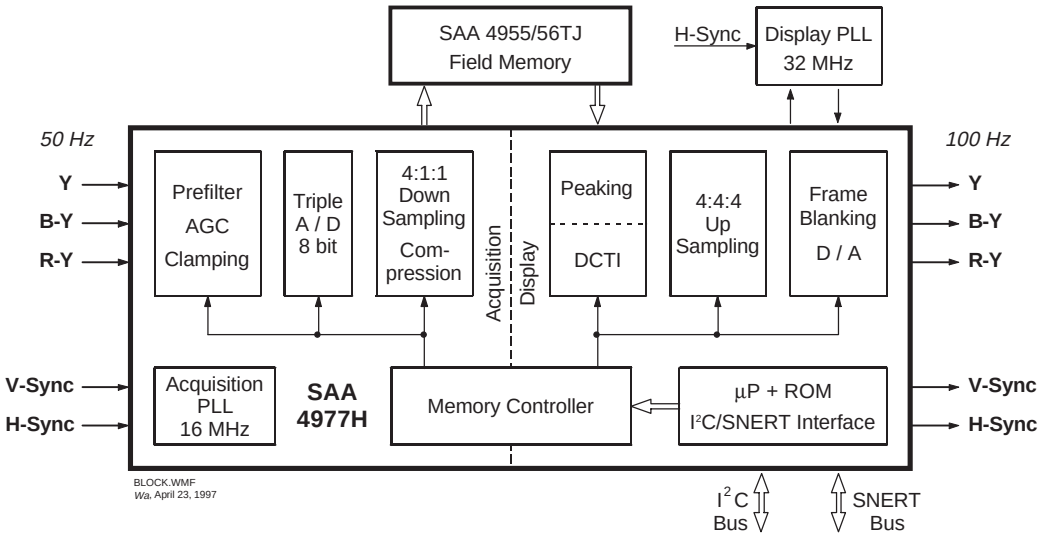
2.1 Description of the different hardware concepts

The SAA 4977 is an IC which allows a very cost-effective design of scan converters. It contains an ADC with clamping function and gain control. The ADC is followed by a signal processing block providing a horizontal compression by the factors 1.17 and 1.33 for 14:9 and 16:9 applications. The data from the compression block is supplied to a field memory. The SAA 4977 also contains a memory controller based on the SAA 4952. An 8051 µ-controller core with ROM is implemented as well. The display datapath provides a high performance digital colour transient improvement and a luminance peaking. In the last block the digital display data are converted into analog signals.

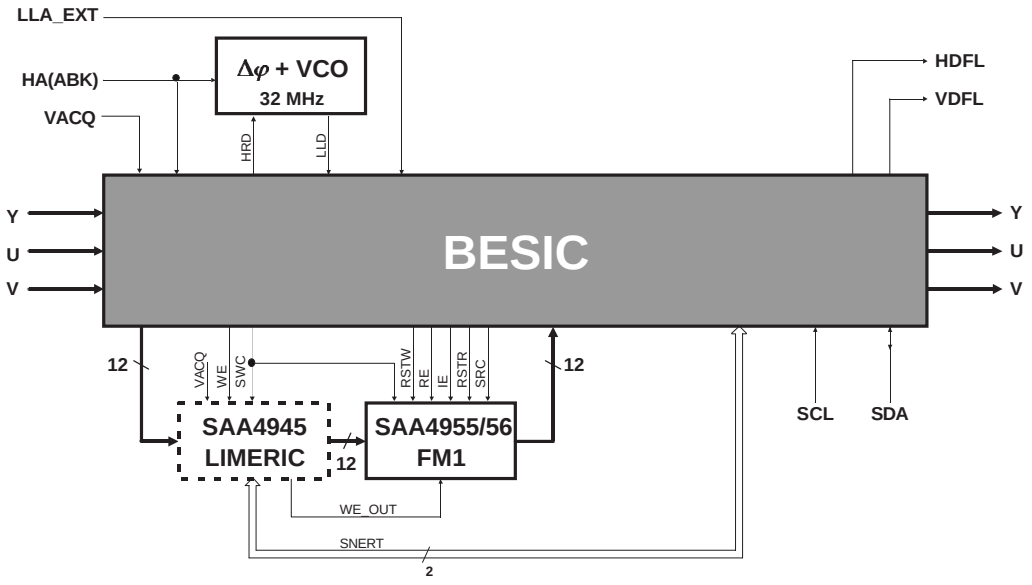
There are different hardware configurations which are supported by the SAA 4977. The low-cost versions only uses one field memory SAA 4955/56. Until the SAA 4956 is finalized the low-cost concept can be upgraded with the LIMERIC (SAA 4945). The mid-range concept is realized with two field memories (SAA 4955) and the PROZONIC (SAA 4990). This concept supports 100 Hz and progressive scan with line flicker reduction, vertical zoom and noise reduction. In the high-end concept the PROZONIC is replaced by the MELZONIC (SAA 4991). This concept provides a vector-based motion compensation for a 100 Hz conversion free of motion effects.

2.2 Block diagrams

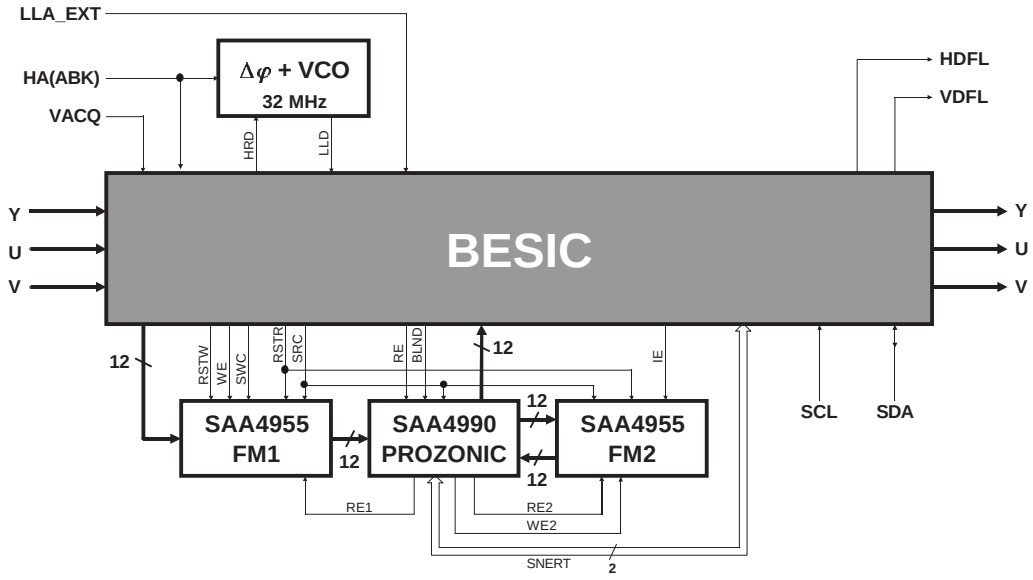
2.2.1 SAA 4977 block diagram



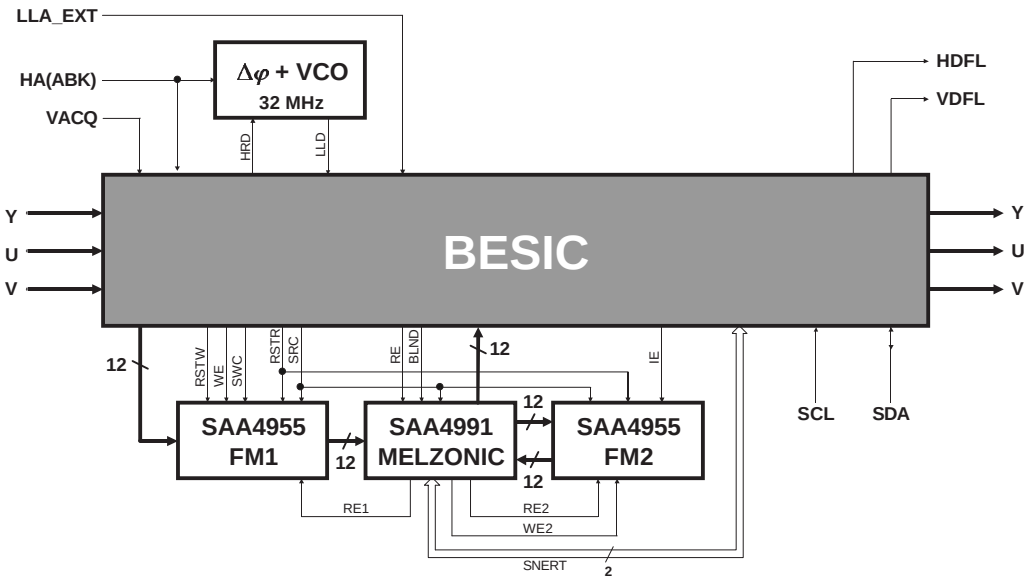
2.2.2 Single field concept



2.2.3 PROZONIC concept



2.2.4 MELZONIC concept



3. I²C-bus interface

3.1 Definition of the interface

The interface of the IPQ µC is realized with a hardware I²C-bus.

The slave address of the IPQ µC is 68h:

Slave address = 0 1 1 0 1 0 0 R/W.

The IPQ µC can either act as a slave receiver or a slave transmitter. In the slave receiver mode the IPQ µC reads I²C register data bytes from the main controller which then acts as a master transmitter. In the slave transmitter mode the IPQ µC sends status information to the main µC which works as a master receiver reading the byte information.

3.2 Sending data to the IPQ µC

3.2.1 I²C transmission protocol

The transmission protocol has the following format:

Start	Slave address 68h	Ack	Subad-dress	Ack	REG1	Ack	.....	Ack	REGx	Ack	Stop

After having addressed the IPQ µC with its slave address the master µC transmits the subaddress plus following register bytes over the I²C-bus. The number of register bytes which are transmitted after the transmission of the subaddress is free choosable. It is possible to transmit just one single register byte after having sent the slaveaddress plus subaddress (3 bytes package).

The IPQ µC acknowledges always all register bytes independent of their contents. If the master µC transmits more than the maximum number of register bytes, the slave µC will acknowledge the following bytes, but will not store them in the internal RAM.

Subaddresses starting from 30h onwards indicate, that datapath control registers are to be serviced.

3.2.2 I²C register tables

[Default hex values in brackets]

TABLE 1 I²C Subaddress 00 hex (FIELD CONTROL) [Default: 60 hex]

Bit	Name	Function
0	PSC	0: Progressive scan mode off 1: Progressive scan mode on
1	G_MODE	0: Generator mode off 1: Generator mode on (312,5 lines / field constantly)
2	FSFM	0: Forced Single Field mode off 1: Forced Single Field mode on
3	SAT	0: Satellite mode off 1: Satellite mode on (A*A*B*B*)
4	A_MOVIE	0: movie detection disabled 1: automatic movie source detection activated; in case a movie mode is detected, a movie will be processed (MOVIE, MOVIE_PHASE are readable via STATUS register)
5	NM	0: Natural Motion mode off 1: Natural Motion mode on
6	LFR	0: Line Flicker Reduction mode off 1: Line Flicker Reduction mode on
7	reserved	

TABLE 2 I²C Subaddress 01 hex [Default: 00 hex]

Bit	Name	Function		
0	MOVIE	0: Forced Movie mode off 1: Forced Movie mode on		
1	PHASE	forced phase flag to be set in combination with MOVIE: 0: normal (ABAB) 1: 180° phase shift (BCBC)		
2	STP	still picture mode: 0: off 1: on (one field out of AABB, full frame median filtered out of LFR)		
3	AFF	acquisition field frequency (50/60 Hz): 0: 50 Hz 1: 60 Hz		
4	COMP0	0: compression off 1: compression on		
5	COMP1	0: 14:9 compression mode 1: 16:9 compression mode		
6	PP0	picture position bit 0		
7	PP1	picture position bit 1		
		PP1	PP0	picture position
		0	0	centre
		0	1	max. left
		1	0	max. right

TABLE 3 I^2C Subaddress 02 hex (VZOOM) [Default: 00 hex]

Bit	Name	Function				
0	VZOOM_0	Vertical zoom bit 0				
1	VZOOM_1	Vertical zoom bit 1				
2	VZOOM_2	Vertical zoom bit 2				
3	VZOOM_3	Vertical zoom bit 3				
		V3	V2	V1	V0	Conversion factor
		0	0	0	0	no zoom
		0	0	0	1	1,06***)**
		0	0	1	0	1,1
		0	0	1	1	1,15***)**
		0	1	0	0	1,2***)**
		0	1	0	1	1,25
		0	1	1	0	1,3***)**
		0	1	1	1	1,33
		1	0	0	0	1,5
		1	0	0	1	reserved
		.	.	.	.	reserved
		1	1	1	1	reserved
4	VCOMPR	Vertical compress				
5	reserved					
6	reserved					
7	INIT	initialize SAA 4977 V1C, PROZONIC/MELZONIC: 0 = off, 1 = on				

*) these zoom-factors are allowed only in the MELZONIC IPQ concept in the LFR or FSFM mode or in the PROZONIC IPQ concept in the PSC mode

TABLE 4 I^2C Subaddress 03 hex (Multi PIP) [Default: 00 hex]

Bit	Name	Function
0	POS0	PIP position bit 0
1	POS1	PIP position bit 1
2	POS2	PIP position bit 2
3	POS3	PIP position bit 3
4	reserved	
5	NPIP	number of PIP‘s 0: 3x3 PIP‘s 1: 4x3 PIP‘s
6	MPIP	0: Multi-PIP off 1: Multi-PIP on
7	SPIP	NTSC PIP: 0: 50 Hz PIP 1: 60 Hz PIP

TABLE 5 I^2C Subaddress 04 hex (NR, SCREEN FADE) [Default: 01 hex]

Bit	Name	Function		
0	NR0	noise reduction bit 0		
1	NR1	noise reduction bit 1		
		NR1	NR0	noise reduction
		0	0	off
		0	1	low
		1	0	middle
		1	1	high
2	SPS0	split screen bit 0		
3	SPS1	split screen bit 1		
		SPS1	SPS0	split screen
		0	X	off
		1	0	horizontal
		1	1	vertical
4	SCF0	screen fade bit 0		
5	SCF1	screen fade bit 1		
		SCF1	SCF0	screen fade
		0	X	off
		1	0	fade in
		1	1	fade out
6	NR_INT	0: normal mode 1: noise reduction processing (bits 1,2) is cancelled each second for the duration of one single display field		
7	PSC_DR	0: normal mode 1: in PROGRESSIVE SCAN mode the display will run in interlace mode		

TABLE 6 I^2C Subaddress 05 hex (HWE DELAY) [Default: 20 hex]

Bit	Name	Function (clock accuracy)
0	HWE1F0	HWE1 fine delay offset to default, bit0
1	HWE1F1	HWE1 fine delay offset to default, bit1
2	HWE1F2	HWE1 fine delay offset to default, bit2
3	HWE1F3	HWE1 fine delay offset to default, bit3
4	HWE1F4	HWE1 fine delay offset to default, bit4
5	HWE1F5	HWE1 fine delay offset to default, bit5
6	HWE1F6	HWE1 fine delay offset to default, bit6
7	HWE1F7	HWE1 fine delay offset to default, bit7

TABLE 7 I²C Subaddress 06 hex (VWE DELAY) [Default: 00 hex]

Bit	Name	Function (line accuracy)
0	VWE1D0	VWE1 delay bit 0
1	VWE1D1	VWE1 delay bit 1
2	VWE1D2	VWE1 delay bit 2
3	VWE1D3	VWE1 delay bit 3
4	VWE1D4	VWE1 delay bit 4
5	VWE1D5	VWE1 delay bit 5
6	VWE1D6	VWE1 delay bit 6
7	A_VSHIFT	0: VSHIFT for VZOOM via I²C Subaddress 06 hex 1: VSHIFT for ZOOM is done automatically in the FSFM mode

TABLE 8 I²C Subaddress 07 hex (BLANK FIELDS) [Default: 80 hex]

Bit	Name	Function		
0	BLANK_F0	Blank field 0		
1	BLANK_F1	Blank field 1		
2	BLANK_F2	Blank field 2		
3	BLANK_F3	Blank field 3		
4	DCD	0: analog colour decoder concept 1: digital colour decoder concept		
5	CON0	IPQ concept bit 0		
6	CON1	IPQ concept bit 1		
		CON1	CON0	IPQ concept
		0	0	Single field concept
		0	1	PROZONIC
		1	X	MELZONIC
7	SFR	0: SFR (VAMSB)=0 1: select field recognition SFR (VAMSB) = 1 This control bit is not active if the PROZONIC hardware concept is selected and the actual chosen field processing is LFR with A_MOVIE set!		

TABLE 9 I^2C Subaddress 08 hex (PORT SETTINGS) [Default: FF hex]

Bit	Name	Function
0	P11	0: clear port bit P1.1 1: set port bit P1.1
1	P12	0: clear port bit P1.2 1: set port bit P1.2
2	P13	0: clear port bit P1.3 1: set port bit P1.3
3	P14	0: clear port bit P1.4 1: set port bit P1.4
4	P15	0: clear port bit P1.5 1: set port bit P1.5
5	reserved	
6	reserved	
7	reserved	

TABLE 10 I^2C Subaddress 09 hex ([Default: 00 hex]

Bit	Name	Function
0	NM_CTL	0: normal mode 1: bad limit taken from I^2C Subaddress 29h reliability threshold taken from I^2C Subaddress 2Ah
1	SET_HOR_DEL	0: normal mode 1: take HOR_DELAYS setting from I^2C Subaddress 26h
2	SET_NR	0: normal mode 1: direct noise reduction control via I^2C Subaddresses 1Fh...25h
3	FILL	0: normal mode 1: fill screen with colour selected via I^2C Subaddress 27h and 28h
4	SET_SIDEP	0: normal mode 1: set SIDEPANEL_START and SIDEPANEL_STOP values direct via I^2C Subaddresses 3Dh and 3Eh
5	VEC_OVL	0: normal mode 1: vector overlay active
6	reserved	
7	SET_VBDA	0: normal mode 1: set VBDASTA/STO values direct via I^2C Subaddresses 0Bh, 0Ch and 0Dh

TABLE 11 I²C Subaddress 0A hex [Default: 00 hex]

Bit	Name	Function
0	SET_HDAV	0: normal mode 1: set HDAVSTA/STO values direct via I²C Subaddresses 0Eh, 0Fh and 16h
1	SET_HBDA	0: normal mode 1: set HBDASTA/STO values direct via I²C Subaddresses 10h, 11h and 16h
2	SET_HRE	0: normal mode 1: set HRESTA/STO values direct via I²C Subaddresses 12h, 13h and 16h
3	SET_HBLND	0: normal mode 1: set HBLNDSTA/STO values direct via I²C Subaddresses 14h, 15h and 16h
4	SET_HDDEL	0: normal mode 1: set HDDEL value direct via I²C Subaddress 17h
5	SET_CLV	0: normal mode 1: set CLVSTA/STO values direct via I²C Subaddresses 18h and 19h
6	SET_HWE	0: normal mode 1: set HWESTA/STO values direct via I²C Subaddresses 1Ah, 1Bh and 0Dh
7	SET_FRG	0: normal mode 1: set HRASTO, HVA_1, HVA_2 and HP1 values direct via I²C Subaddresses 1Ch, 1Dh,1Eh and 2Bh

TABLE 12 I²C Subaddress 0B hex (VBDASTA) [Default: 15 hex]

Bit	Name	Function
0....7	VBDASTA	direct memory controller register access

TABLE 13 I²C Subaddress 0C hex (VBDASTO) [Default: 31 hex]

Bit	Name	Function
0....7	VBDASTO	direct memory controller register access

TABLE 14 I²C Subaddress 0D hex (MSBREG1) [Default: 0A hex]

Bit	Name	Function
0	MSB_ VBDASTA	direct memory controller register access
1	MSB_ VBDASTO	direct memory controller register access
2	MSB_ HWESTA	direct memory controller register access
3	MSB_ HWESTO	direct memory controller register access
4....7	reserved	

TABLE 15 I²C Subaddress 0E hex (HDAVSTA) [Default: 28 hex]

Bit	Name	Function
0.... 7	HDAVSTA	direct memory controller register access

TABLE 16 I²C Subaddress 0F hex (HDAVSTO) [Default: 00 hex]

Bit	Name	Function
0.... 7	HDAVSTO	direct memory controller register access

TABLE 17 I²C Subaddress 10 hex (HBDASTA) [Default: 55 hex]

Bit	Name	Function
0.... 7	HBDASTA	direct memory controller register access

TABLE 18 I²C Subaddress 11 hex (HBDASTO) [Default: EE hex]

Bit	Name	Function
0.... 7	HBDASTO	direct memory controller register access

TABLE 19 I²C Subaddress 12 hex (HRESTA) [Default: 3A hex]

Bit	Name	Function
0.... 7	HRESTA	direct memory controller register access

TABLE 20 I²C Subaddress 13 hex (HRESTO) [Default: DE hex]

Bit	Name	Function
0.... 7	HRESTO	direct memory controller register access

TABLE 21 I²C Subaddress 14 hex (HBLNDSTA) [Default: 00 hex]

Bit	Name	Function
0.... 7	HBLNDSTA	direct memory controller register access

TABLE 22 I²C Subaddress 15 hex (HBLNDSTO) [Default: 00 hex]

Bit	Name	Function
0.... 7	HBLNDSTO	direct memory controller register access

TABLE 23 I²C Subaddress 16 hex (MSB REG2) [Default: 2A hex]

Bit	Name	Function
0	MSB_ HDAVSTA	direct memory controller register access
1	MSB_ HDAVSTO	direct memory controller register access
2	MSB_ HBDASTA	direct memory controller register access
3	MSB_ HBDASTO	direct memory controller register access
4	HRESTA	direct memory controller register access
5	HRESTO	direct memory controller register access
6	MSB_ HBLNDSTA	direct memory controller register access
7	MSB_ HBLNDSTO	direct memory controller register access

TABLE 24 I²C Subaddress 17 hex (HDDEL) [Default: 00 hex]

Bit	Name	Function
0	HDDEL	fine delay of HDAV
1		fine delay of HBDA
2		fine delay of HRE
3		fine delay of HBLND
4.... 7	reserved	

TABLE 25 I²C Subaddress 18 hex (CLVSTA) [Default: 00 hex]

Bit	Name	Function
0.... 7	CLVSTA	direct memory controller register access

TABLE 26 I²C Subaddress 19 hex (CLVSTO) [Default: 09 hex]

Bit	Name	Function
0.... 7	CLVSTO	direct memory controller register access

TABLE 27 I²C Subaddress 1A hex (HWESTA) [Default: 2C hex]

Bit	Name	Function
0.... 7	HWESTA	direct memory controller register access

TABLE 28 I²C Subaddress 1B hex (HWESTO) [Default: D0 hex]

Bit	Name	Function
0.... 7	HWESTO	direct memory controller register access

TABLE 29 I²C Subaddress 1C hex (HRASTO) [Default: 80 hex]

Bit	Name	Function
0....7	HRASTO	direct memory controller register access

TABLE 30 I²C Subaddress 1D hex (HVA_1) [Default: 28 hex]

Bit	Name	Function
0....7	HVA_1	direct memory controller register access

TABLE 31 I²C Subaddress 1E hex (HVA_2) [Default: A8 hex]

Bit	Name	Function
0....7	HVA_2	direct memory controller register access

TABLE 32 I²C Subaddress 1F...25 hex

Subaddress (hex)	Name	Function
1F	KSTEP01	direct PROZONIC/MELZONIC register access (default: 34 hex)
20	KSTEP23	direct PROZONIC/MELZONIC register access (default: 34 hex)
21	KSTEP45	direct PROZONIC/MELZONIC register access (default: 34 hex)
22	KSTEP67	direct PROZONIC/MELZONIC register access (default: 34 hex)
23	KFIXED	direct PROZONIC/MELZONIC register access (default: 8F hex)
24	TFILTER12	direct PROZONIC/MELZONIC register access (default: 55 hex)
25	DEF	direct PROZONIC register access (default: 09 hex) direct MELZONIC register access (default: 00 hex)

TABLE 33 I²C Subaddress 26 hex (HOR_DELAYS) [Default: 28 hex]

Bit	Name	Function
0....7	HOR_ DELAYS	direct PROZONIC/MELZONIC register access

TABLE 34 I²C Subaddress 27 hex (FIXCOL_Y) [Default: 16 hex]

Bit	Name	Function
0....7	FIXCOL_Y	direct MELZONIC register access

TABLE 35 I²C Subaddress 28 hex (FIXCOL_UV) [Default: 08 hex]

Bit	Name	Function
0....7	FIXCOL_UV	direct MELZONIC register access

TABLE 36 I²C Subaddress 29 hex (BAD_LIMIT) [Default: 40 hex]

Bit	Name	Function
0....7	BAD_LIMIT	direct BAD_LIMIT setting (Software threshold for NR_BAD_RANGES, MELZONIC control)

TABLE 37 I²C Subaddress 2A hex (RELIABILITY_SEL) [Default: 30 hex]

Bit	Name	Function
0....7	RELIABILITY_SEL	direct MELZONIC register access

TABLE 38 I²C Subaddress 2B hex (HP1) [Default: A8 hex]

Bit	Name	Function
0....7	HP1	direct memory controller register access; the control values of the pulses HP2, HP3 and HP4 are automatically adapted that the distance of the 4 HP pulses is 40 Hex (=16 us)

TABLE 39 I²C Subaddress 2C hex (LIMERIC1) [Default: 00 hex]

Bit	Name	Function			
0	L_NR0	LIMERIC Noise Reduction bit0			
1	L_NR1	LIMERIC Noise Reduction bit1			
2	L_NR2	LIMERIC Noise Reduction bit2			
		L_NR0	L_NR1	L_NR2	
		0	0	0	Noise-Reduction off
		0	0	1	Noise-Reduction low
		0	1	0	Noise-Reduction middle
		0	1	1	Noise-Reduction high
		1	0	0	Noise-Reduction highest
3	DEM	0: normal mode 1: demo mode			
4	WES	0: normal mode 1: shift write enable for one clock			
5	EX_THR	0: internal threshold 1: set threshold value direct via I²C Subaddress 2Dh			
6	reserved				
7	reserved				

TABLE 40 I²C Subaddress 2D hex (LIMERIC2) [Default: 00 hex]

Bit	Name	Function
0....7	NTHR	direct LIMERIC register access

TABLE 41 I²C Subaddress 2E hex (LIMERIC3) [Default: 0F hex]

Bit	Name	Function
0....7	WVAL	direct LIMERIC register access

I2C Translator Registers

TABLE 42 I²C Translator Subaddress 30 hex (ACQ_0) [Default: 66 hex]

Bit	Name	Host Address	Default	Function
0....7	AGC_Y	150 hex	66 hex	AGC gain for the Y channel (2's complement rel 0dB): upper 8 bits

TABLE 43 I²C Translator Subaddress 31 hex (ACQ_1) [Default: 90 hex]

Bit	Name	Host Address	Default	Function
0....7	AGC_UV	151 hex	90 hex	AGC gain for the U and V channel (2's complement rel 0dB): upper 8 bits

TABLE 44 I²C Translator Subaddress 32 hex (ACQ_2) [Default: 00 hex]

Bit	Name	Host Address	Default	Function
0	AGC_Y_LSB	152 hex	00 hex	AGC gain for Y channel LSB
1	AGC_UV_LSB			AGC gain for UV channel LSB
2	standby_f			1: frontend in stand-by mode
3	aaf_bypass			1: bypass for prefilter
4....7	reserved			

TABLE 45 I²C Translator Subaddress 33 hex (ACQ_3) [Default: 00 hex]

Bit	Name	Host Address	Default	Function		
0....1	UVclcorrect_mode	153 hex	00	Bit1	Bit 0	UV clamp mode
				0	0	auto
				0	1	fixed
				1	0	keep
				1	1	-
2....4	Uclcorrect_fval		000	fixed value clamp corr. U channel (2's complement)		
5....7	Vclcorrect_fval		000	fixed value clamp corr. V channel (2's complement)		

TABLE 46 I²C Translator Subaddress 34 hex (ACQ_4) [Default: 30 hex]

Bit	Name	Host Address	Default	Function		
0....1	UVcoring	154 hex	00	Bit1	Bit0	UV coring level
				0	0	0
				0	1	+/- 0,5
				1	0	+/- 1
				1	1	+/- 2
2	reserved		0			
3	reserved		0			
4....5	UVcl_tau		11	Bit1	Bit0	vertical filtering of measured clamp
				0	0	
				0	1	
				1	0	
				1	1	
6	reserved		0			
7	reserved		0			

TABLE 47 I²C Translator Subaddress 35 hex (ACQ_5) [Default: 0A hex]

Bit	Name	Host Address	Default	Function			
0....2	Ydelay_f	155 hex	010	Bit2	Bit1	Bit0	variable Y-delay
				0	0	0	-4
				0	0	1	-3
				0	1	0	-2
				0	1	1	-1
				1	0	0	0
				1	0	1	1
				1	1	0	2
				1	1	1	3
3....4	overl_thr		01	Bit1	Bit0	overload threshold	
				0	0	216	
				0	1	224	
				1	0	232	
				1	1	240	
5	fill_mem		0	0: standard mode, video data from the ADC 1: fill memory with constant value			
6	reserved		0				
7	reserved		0				

TABLE 48 I²C Translator Subaddress 36 hex (DCTI_0) [Default: 82 hex]

Bit	Name	Host Address	Default	Function			
0....2	dcti_gain	1D1 hex	010	Bit2	Bit1	Bit0	DCTI gain
				0	0	0	0
				0	0	1	1
				0	1	0	2
				0	1	1	3
				1	0	0	4
				1	0	1	5
				1	1	0	6
				1	1	1	7
3....6	dcti_ threshold		0000	DCTI threshold (0, 1, 2,...., 14, 15)			
7	dcti_ddx_sel		1	DCTI ddx_sel 0: low 1: high			

TABLE 49 I²C Translator Subaddress 37 hex (DCTI_1) [Default: 3E hex]

Bit	Name	Host Address	Default	Function		
0....1	dcti_limit	1D2 hex	10	Bit1	Bit0	DCTI limit
				0	0	0
				0	1	1
				1	0	2
				1	1	3
2	dcti_separate		1	0: off 1: on		
3	dcti_ protection		1	0: off 1: on		
4	dcti_filteron		1	0: off 1: on		
5	dcti_superhill		1	0: off 1: on		
6	reserved		0			
7	reserved		0			

TABLE 50 I^2C Translator Subaddress 38 hex (PEAK_0) [Default: 12 hex]

Bit	Name	Host Address	Default	Function			
0....2	pk_alpha	1D3 hex	010	Bit2	Bit1	Bit0	peaking alpha
				0	0	0	0
				0	0	1	1/16
				0	1	0	2/16
				0	1	1	3/16
				1	0	0	4/16
				1	0	1	5/16
				1	1	0	6/16
				1	1	1	8/16
3....5	pk_beta		010	Bit2	Bit1	Bit0	peaking beta
				0	0	0	0
				0	0	1	1/16
				0	1	0	2/16
				0	1	1	3/16
				1	0	0	4/16
				1	0	1	5/16
				1	1	0	6/16
				1	1	1	8/16
6	reserved		0				
7	reserved		0				

TABLE 51 I²C Translator Subaddress 39 hex (PEAK_1) [Default: 02 hex]

Bit	Name	Host Address	Default	Function			
0....2	pk_tau	1D4 hex	010	Bit2	Bit1	Bit0	peaking tau
				0	0	0	0
				0	0	1	1/16
				0	1	0	2/16
				0	1	1	3/16
				1	0	0	4/16
				1	0	1	5/16
				1	1	0	6/16
				1	1	1	8/16
3....4	pk_delta		00	Bit1	Bit0	peaking delta	
				0	0	0	
				0	1	1/16	
				1	0	2/16	
				1	1	4/16	
5....6	pk_neggain		00	Bit1	Bit0	peaking negative gain	
				0	0	0	
				0	1	1/16	
				1	0	2/16	
				1	1	4/16	
7	reserved		0				

TABLE 52 I²C Translator Subaddress 3A hex (PEAK_2) [Default: 02 hex]

Bit	Name	Host Address	Default	Function
0....3	pk_corthr	1D5 hex	0010	peaking coring threshold (0,8,16,...,120)
4	reserved		0	
5	reserved		0	
6	reserved		0	
7	reserved		0	

TABLE 53 I²C Translator Subaddress 3B hex (SIDEP_OVL_UV) [Default: 28 hex]

Bit	Name	Host Address	Default	Function
0....3	overlay_U	1D6 hex	1000	sidepanel overlay U (4 upper bits, 2's complement)
4....7	overlay_V		0010	sidepanel overlay V (4 upper bits 2's complement)

TABLE 54 I²C Translator Subaddress 3C hex (SIDEP_OVL_Y) [Default: 4E hex]

Bit	Name	Host Address	Default	Function
0....7	overlay_Y	1D7 hex	4E hex	sidepanels overlay Y (8 upper bits)

TABLE 55 I²C Translator Subaddress 3D hex (RIGHT_SIDEP) [Default: FB hex]

Bit	Name	Host Address	Default	Function
0....7	sidepanel_ start	1D8 hex	FB hex	right sidepanel position (8 upper bits)

TABLE 56 I²C Translator Subaddress 3E hex (LEFT_SIDEP) [Default: 28 hex]

Bit	Name	Host Address	Default	Function
0....7	sidepanel_ stop	1D9 hex	00 hex	left sidepanel position (8 upper bits)

TABLE 57 I²C Translator Subaddress 3F hex (SIDEP_FDEL) [Default: 70 hex]

Bit	Name	Host Address	Default	Function			
0....1	sidepanel_ fdel	1DA hex	00	Bit1	Bit0	sidepanel fine delay	
				0	0	0	
				0	1	1	
				1	0	2	
				1	1	3	
2	output_range		0	Y output range 0: 9bit, blanking level 288 1: 10bit, blanking level 64			
3	UV_inv		0	0: default 1: invert UV input			
4....6	Ydelay_b		111	Bit2	Bit1	Bit0	variable Y-delay
				0	0	0	-7
				0	0	1	-6
				0	1	0	-5
				0	1	1	-4
				1	0	0	-3
				1	0	1	-2
				1	1	0	-1
				1	1	1	0
7	reserved		0				

3.3 Receiving data from the IPQ µC

The IPQ µC is able to transmit one status byte plus additional read bytes to the main µC. The IPQ µC then works as a slave transmitter.

The I^2C-bus transmission protocol for transmitting the status byte plus read registers has the following format:

Start	Slave address 69h	Ack	Status byte	ReadReg1	Ack	...	Nack	Stop

3.3.1 Content of status register

The status register contains the following information:

TABLE 58 I^2C Read Register 01 hex (STATUS) No Subaddress!

Bit	Name	Default	Function
0	NON_IL	0	0: non interlace mode not active 1: non interlace mode active
1	FEATURE_ MODE	0	0: no feature mode detected 1: feature mode detected
2	AUTO_ MOVIE_FLAG	0	0: normal mode 1: automatic movie mode activated
3	MOVIE_ FLAG	0	0: no movie source detected 1: movie detected
4	PHASE_ FLAG	0	0: standard mode (ABAB in case of MOVIE=1) 1: 180° phase shift (BCBC in case of MOVIE=1)
5	SCREEN_ FADE_ACTIVE	0	0: screen fade not active 1: screen fade active
6	READY	0	0: not ready to accept I^2C commands 1: ready to accept I^2C commands
7	WATCH	0	Watchdog bit; will be toggled when status byte is read by master µC, initialized with 0

3.3.2 Content of the following Read Registers

TABLE 59 I^2C Read Register 02 hex (SCREEN_FADE_COUNT) No Subaddress!

Bit	Name	Function
0.... 7	SCREEN_FADE_COUNT	00: fade activity starts 01..FE hex: fade positions FF: fade activity completed

TABLE 60 I²C Read Register 03 hex (MPD MSByte1) No Subaddress!

Bit	Name	Function
0.... 7	MOVIE_PHASE_A	direct PROZONIC/MELZONIC register read, MSByte; Movie phase detection byte 1

TABLE 61 I²C Read Register 04 hex (MPD MSByte2) No Subaddress!

Bit	Name	Function
0.... 7	MOVIE_PHASE_B	direct PROZONIC/MELZONIC register read, MSByte; Movie phase detection byte 2

TABLE 62 I²C Read Register 05 hex (read_Uclerror) No Subaddress!
(not available for digital acquisition concept)

Bit	Name	Host Address	Function
0.... 6	read_Uclerror	170 hex	read U channel clamp error (range: +3/-4 bit; resolution: 1/16 bit)
7	reserved		

TABLE 63 I²C Read Register 06 hex (read_Vclerror) No Subaddress!
(not available for digital acquisition concept)

Bit	Name	Host Address	Function
0.... 6	read_Vclerror	171 hex	read V channel clamp error (range: +3/-4 bit; resolution: 1/16 bit)
7	reserved		

TABLE 64 I²C Read Register 07 hex (read_Ygain) No Subaddress!
(not available for digital acquisition concept)

Bit	Name	Host Address	Function
0.... 7	read_Ygain	172 hex	read overflow indication of Y channel

TABLE 65 I²C Read Register 08 hex (AGC_Y_read) No Subaddress!
(not available for digital acquisition concept)

Bit	Name	Host Address	Function
0.... 7	AGC_Y_read	173 hex	AGC gain for Y channel, upper 8 bits (for functional test only)

TABLE 66 I^2C Read Register 09 hex (SOFTWARE_VERSION) No Subaddress!

Bit	Name	Function
0.... 7	SOFTWARE_VERSION	10 hex

3.4 Timing aspects

The maximum allowed response time between accepting register bytes and the execution of the commands handled by the IPQ µC is 90 ms. This time is only relevant when field memory control modes are changed. Field memory control modes are: AABB, Natural Motion, Movie, LFR, Still, Multi-PIP mode (see table 73). When a new field memory control mode has been chosen via I^2C the IPQ µC waits max. 40 ms until the new processing starts.

The maximum allowed total clock stretch time of the IPQ µC within one I^2C message is 5 ms.

The minimum wait time between sending two I^2C bus register data packages varies from 12 ms (no field memory control modes have changed) to 90 ms (field memory control modes have changed).

If the user wants to make sure that a complete I^2C bus register data package is transmitted without being interrupted by a VDFL interrupt request routine and the slave µC is free for I^2C after the master µC transmits I^2C data, the I^2C data package should be transmitted between 3 and 5 ms after VDFL occurred. The slave µC sets bit 6 of the status byte when it is ready to accept I^2C commands.

Multi-PIP:

The time between one live PIP picture register command to another should not be shorter than 120 ms.

Screen fade:

As long as this mode is active all other mode changes are ignored. As long as the screen fade processing has not finished the control bit SCREEN_FADE_ACTIVE in the status byte is set.

4. Evaluation of I^2C-bus register data

4.1 Field Memory Control Modes

The main functionality is listed in the table below dependent on the chosen hardware concept.

Table 67: Control Modes

	Concept		
Field Control Modes	Melzonic	Prozonic	Single Field
AABB	x	x	x
LFR	x	x	-
NM Natural Motion for Video and Movie	x	-	-
ABAB Movie	x	x	-
Sat-Mode	x	x	-
PSC	x	x	-
G_MODE Genera-tor Mode	x	x	x
MPIP	x	x	-
FSFM Forced Single Field Mode	x	x	x
VZOOM	x	x	-
FSFM in progr. scan	x	x	-
PHASE for Movie	x	x	-
STILL	x	x	x

Table 67: Control Modes

	Concept		
Field Control Modes	**Melzonic**	**Prozonic**	**Single Field**
NON_IL	x	x	x

The following section describes the field memory control modes of the SAA4977 and additional functions which can be controlled via I^2C bus. The priority of the command bits can be derived from the flow charts for the different hardware concepts in chapter 3.1.2.

4.1.1 AABB Mode

Software control: Mode with the lowest priority (all other field control bits switched off).

The AABB mode is the most simple conversion mode for 100 Hz. Only one field memory is implemented. The video data of an incoming field are simply doubled in an AABB sequence. For the low-end 100 Hz concept this mode is the default conversion mode.

This mode can also be used in the PROZONIC and MELZONIC concept. The mode even has to work correctly if the PROZONIC and MELZONIC is removed. This demand means that the vertical display read control is realized via the memory controller part of SAA 4977 and not by the VRE control of the external processing ICs. In the live AABB mode the DR-Bit (VDFL delay of 0.5 lines) is toggled field by field to generate the AABB raster with the field length sequence 313, 312.5, 312 and 312.5 lines.

4.1.2 LFR Mode

Software Control: I^2C-Register subaddress 0 hex, Bit 6 (LFR)

The Line Flicker Reduction (LFR) mode is the default control mode of the PROZONIC concept and can be used in combination with MELZONIC as well. It makes use of a medianfilter to generate the output sequence: original field A, medianfiltered A*, medianfiltered B* and original field B.

4.1.3 Natural Motion (Video and Movie)

Software Control: I^2C-Register subaddress 0 hex, Bit 5 (NM)

This function can only be realized in the high-end Melzonic concept. The MELZONIC will compensate movement artefacts which are caused by e.g. simple field doubling in the 100 Hz mode. For video sources with 50 Hz motion resolution a constant 100 Hz motion is calculated by a vector based motion estimation and compensation. For movie sources which have a motion resolution of only 25 Hz the MELZONIC is able to increase the motion frequency to 50 Hz. This provides a remarkable improvement for the display of movies even compared to 50 Hz standard TVs.

A recursive block matching algorithm is implemented in the SAA 4991. Beside the simple field control of the above described two natural motion modes the software has to check the quality of the

motion compensation. The µC in the SAA 4977 reads the MELZONIC register NR_BAD_RANGES. It contains the information in how many ranges of the field the vector compensation has failed. This register will be compared with a free definable constant BAD_LIMIT. Every time NR_BAD_RANGES is greater than BAD_LIMIT for a defined number of fields the MELZONIC control bits FC_RLLBCK will be cleared. This means that the vector information is no longer used for the field processing. The converter is switched into a fallback mode. The fallback mode depends on the field control bits setting. It is a control mode with a lower priority, in which no vector based processing is performed. If NR_BAD_RANGES is smaller than BAD_LIMIT the vector based natural motion processing will be activated after a delay of some fields. The value of FC_RLLBCK is set to 4. The vector information is used and a motion compensated display is generated. The comparison of NR_BAD_RANGES with BAD_LIMIT allows a global control of the natural motion under quality aspects. The maximum allowed estimation error (SAD) within a block can be controlled via the register reliability-threshold. This register setting influences the local behaviour of the processing additionally.

As mentioned above the natural motion processing has to be adapted to the motion resolution of the source. For this requirement it is necessary to detect if a movie or a video source has to be motion compensated (see chapter 4.1.7). The correct mode (video or movie processing) can be controlled by the user himself or by an automatic routine.

4.1.4 ABAB Movie Mode

Software Control: I^2C-Register subaddress 1hex, Bit 0 (MOVIE) and Bit 1 (PHASE)

This mode is supported by the PROZONIC and MELZONIC approach. The converter performs a frame repetition. The phase relation between the movie pictures and the incoming video signal is not standardized. Via the additional control bit PHASE (I^2C-Register subaddress 1 hex, bit 1) the processing is put into the correct phase relation to the incoming movie (ABAB or BCBC).

4.1.5 Satellite Mode

Software Control: I^2C-Register subaddress 0 hex, Bit 3 (SAT)

In the satellite mode all the four 100 Hz display fields are derived from the output of the median filter. The median filter will filter out details occurring in only one line. This fact can be used to attenuate typical FM noise dropouts which normally occur uncorrelated in the field. A bad satellite signal reception can be improved quite effectively in this mode without deteriorating the picture quality.

4.1.6 Progressive Scan Mode (PSC)

Software Control: I^2C-Register subaddress 0 hex, Bit 0 (PSC)

If the bit PSC is set a progressive scan mode is activated. The de-interlacing function (line interpolation) is performed with the help of the median filter of PROZONIC or MELZONIC. This mode is preferable for NTSC sources. The number of lines per field (525 lines / 60 Hz) is doubled and additionally the line flicker is removed. For NTSC sources this reduction of the visibility of the line structure is more important than the reduction of large area flicker (60/120 Hz) because a 60 Hz display is much less flickering compared to a 50 Hz display.

The progressive scan display can also been displayed interlaced if the bit PSC_DR (I^2C-Register subaddress 4 hex, bit 7 is set. In this case a line-flicker becomes visible but the number of displayed lines is doubled (1250 lines for PAL and 1050 lines for NTSC).

4.1.7 Generator Mode (G_Mode)

Software Control: I^2C-Register subaddress 0 hex, Bit 1 (G_MODE)

The bit G_MODE activates a stable 100 Hz display with a fixed field length of 312.5 lines for AFF=0 and 262.5 lines for AFF=1. The display field length is not adapted according to the video source. The conversion mode is reduced to a single field repetition mode (AAAA). This special mode can be used to get a stable OSD picture without a source or with a very noisy source. It does also improve the picture stability for a tuner channel search.

4.1.8 Auto Movie Detection routine

Software Control: I^2C-Register subaddress 0 hex, Bit 4 (A_MOVIE)

Auto Movie Detection in the Melzonic concept

The bit A_MOVIE activates an automatic movie source detection if the natural motion mode is switched on (NM=1). The detection is based on the read values of the MELZONIC registers “vector_sum”. This sum of vector absolutes represents the amount of motion found between two incoming fields. The software investigates the vector sums of a whole frame to detect whether a video or a movie source is connected. If the two values show a large difference the converter can be switched to a vector based movie processing increasing the movement resolution from 25 Hz to 50 Hz. The annoying motion judder of movies is eliminated. The phase relation between the movie pictures and the video fields is taken into account. In case of a video source or scenes with no or small motion the video processing is active, increasing the movement resolution from 50 Hz to 100 Hz. This removes the unsharpness of moving edges compared to a simple field repetition 100 Hz converter.

If the A_MOVIE bit is set to zero, the converter is performing a motion compensation processing for video sources as long as the bit MOVIE is cleared. If MOVIE is set a movie motion compensation is activated. The phase relation to the incoming movie can be adapted via the control bit PHASE. The user is able to adapt the natural motion processing to the source via the bits MOVIE and PHASE by himself if the automatic movie detection routine has been switched off.

Auto Movie Detection in the Prozonic concept

If the bit A_MOVIE is set in the PROZONIC concept the same routine as described above will investigate whether a movie source is applied and in which phase relation it is transmitted. The software uses the PROZONIC read register MPD to get a motion information which is not based on a vector sum but on a sum of absolute differences in the luminance channel. With PROZONIC the movie detection is not used to activate a movie mode. The LFR sequence AA*B*B is adapted to the phase of a movie and can be switched to a BB*C*C processing automatically. This results in an improved performance of vertical rolling titles. The time constant of the Auto Movie routine is increased compared to the MELZONIC approach. There is no need for a fast detection because no

severe artefacts occur if the detection has a delay. The control bit SFR can not be controlled by the user as long the bit A_MOVIE is set in the PROZONIC LFR mode.

4.1.9 Multi-PIP (MPIP)

Software Control: I^2C-Register subaddress 3 hex, Bit 6 (MPIP)

The field memories of the 100 Hz converter can be used to generate a MPIP picture if MPIP is set. It is assumed that the TV set contains a PIP Module which generates a compressed PIP picture at the bottom right corner of the screen. The picture supplied by the PIP module is written into the field memories and placed according to the chosen position of the MPIP control (I^2C-Register subaddress 3 hex, POS0-POS3). The complete MPIP picture shows 3 x 3 or 4 x 3 small pictures. One of those can display a live source, the others are frozen. With the control bit SPIP (I^2C register 3, bit 7) the PIP window can be adapted to a 60 Hz PIP source. The vertical size of the PIP window is reduced if SPIP is set.The MPIP feature makes use of the boxing function of PROZONIC or MELZONIC. The noise reduction circuitry (k-factor control) together with the defined boxes support the PIP function. The MPIP feature can be used for a channel overview or to show frozen motion phases of one channel (photo finish).

4.1.10 Forced Single Field Mode (FSFM)

Software Control: I^2C-Register subaddress 0 hex, bit 2

In the forced single field mode only one field of a frame is displayed four times (AAAA). The advantage of this mode is that the vertical zoom factor and the displayed part of the picture can be changed without picture distortions. This mode is activated via the control bit FSFM. The mode is used automatically, if the software detects a non-standard source. If the field length of the incoming source differs more than 3 lines from a standard source (PAL 312.5/NTSC 262.5 lines per field) the single field mode is activated. This improves the picture performance for VCR in trick modes.

In Progressive Scan there is also supported a single field mode. In this case the lines of a field are simply doubled. This progressive output field is displayed twice per input frame (AA).

4.1.11 Vertical Zoom

Software Control: I^2C-Register subaddress 2 hex (VZOOM)

A vertical zoom function realized by an interpolation of lines can be activated via the I^2C register VZOOM. The zoom factor is defined by the control bits VZOOM_0 to VZOOM_3. The factors 1.1, 1.25, 1.33 and 1.5 are fully supported by the control software. The zoom function can be combined with the LFR and the natural motion feature (video and movie source). If the AABB mode is chosen together with vertical zoom the module switches automatically to a LFR processing. In the MELZONIC concept in the LFR and FSFM mode additional zoom factors are supported (1.06, 1.15, 1.2, 1.3). These factors are supported as well in the PROZONIC concept in the PSC mode. The 5 percent steps in the vertical zoom factor allow a smooth change of the zoom mode with several intermediate steps (see FSFM Mode).

4.1.12 Vertical Compression

Software Control: I^2C-Register subaddress 2, bit 4 (VCOMPR)

In the progressive scan mode a vertical compression factor of 0.8 is supported for the MELZONIC and PROZONIC concept. This mode allows to display a PAL source on an LCD or Plasma display foreseen for an NTSC source.

4.1.13 Still Picture Mode

Software Control I^2C Register subaddress 1 hex, bit 2 (STP)

The Still Picture function can be combined with every conversion mode. For the modes LFR and Natural Motion the frozen picture is processed based on a frame displaying the original field A and the median filtered field A*. In the AABB mode, MPIP, SAT Mode and Generator Mode only a one field still picture is generated. In the MOVIE mode (ABAB) a complete frame is displayed in the Still Mode. In Progressive Scan also a frame based still picture is displayed consisting of original lines and median filtered lines.

4.1.14 Non-Interlace Mode

Software Control: no I^2C control

If a non-interlace source is detected by the software the field processing switches automatically into a Non-Interlace Mode. The detection criteria is a field length which is N complete lines. As the memory controller counts half lines starting with zero a non-interlace source will set the LSB of the field length read register (PAL standard = 270 hex, NTSC standard = 20C hex). A non-interlace source is additionally indicated in bit 0 of the status read register (NON_IL).

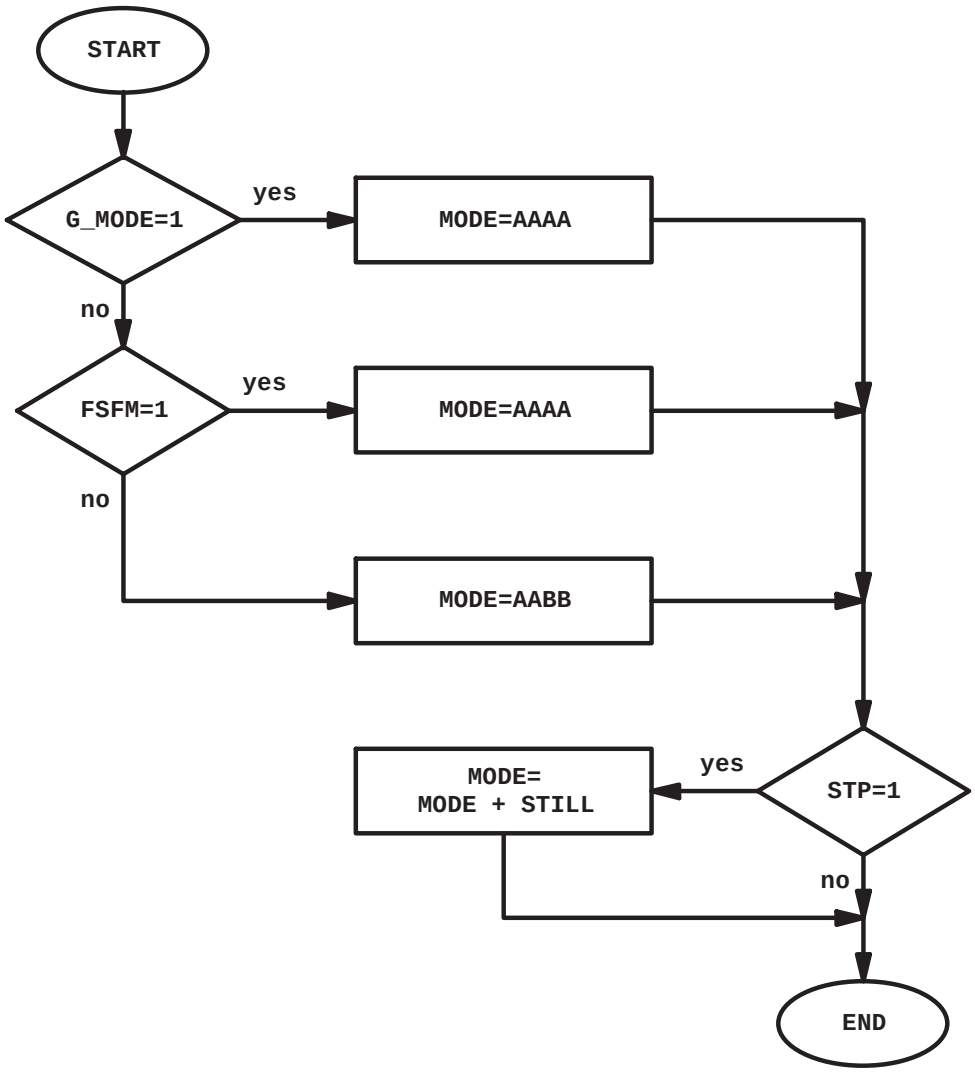
4.1.15 INIT

Software Control I^2C Register subaddress 2 hex, bit 7 (INIT)

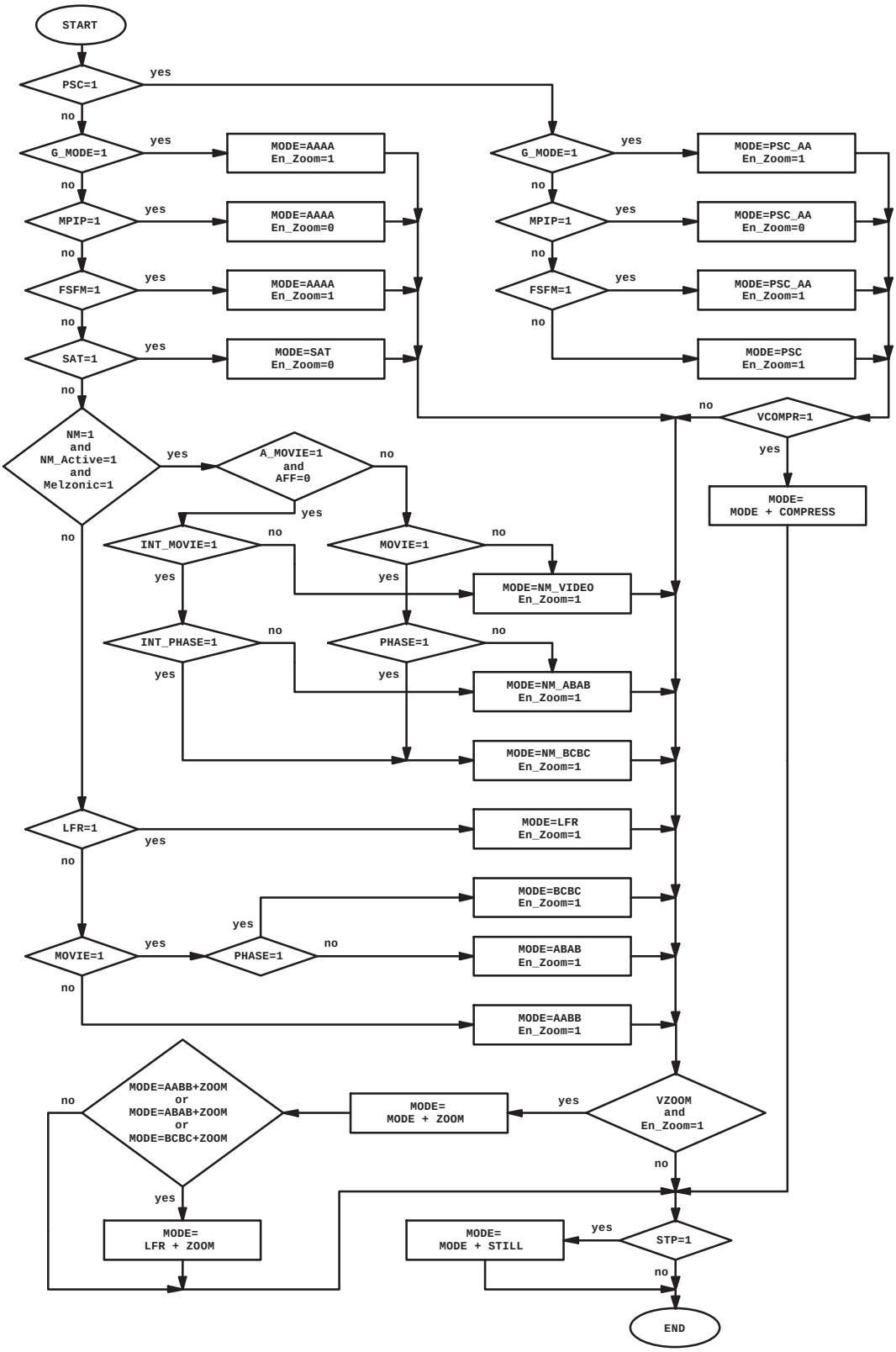
If the Init bit is set the SAA 4977 module will be initialized with the default values. The initialization settings of the software are supporting the single field concept (AABB mode). If another IPQ hardware concept is used it has to be defined via the control bits CON0 and CON1 afterwards.

4.2 Priorities of field memory control modes

4.2.1 Single field memory concept



4.2.2 Two field memory concepts



4.3 Secondary control commands

The secondary control commands can be combined with the above described field control modes.

4.3.1 Memory control of the SAA 4977 V1C

Acquisition Field Frequency selection (AFF)

Software Control I^2C Register subaddress 1 hex, bit 3 (AFF)

The bit AFF is set by the user according to the vertical frequency of the incoming source. In case of a 50 Hz source the bit is cleared, for 60 Hz sources it is set. The vertical writing window is adapted (VWE1STA and VWE1STO). The bit also changes the reference field length for the feature mode detection (see FSFM mode). In the generator mode the field length is set to 312.5 lines for AFF=0 and 262.5 lines for AFF=1.

HWE Delay

Software Control: I^2C-Register subaddress 5 hex, (HWE1F0 to HWE1F7)

The horizontal writing window can be delayed via the I^2C register HWE Delay. The step width of the delay has clock accuracy.

VWE Delay

Software Control: I^2C-Register subaddress 6 hex, VWE1D0 - VWE1D6

The vertical writing window can be delayed in steps of lines via the I^2C register VWE Delay.

The possible delay range is 0 to127 lines. The delay function is needed to centre a vertical zoomed picture. In the field control mode FSFM the picture is automatically centred if the control bit A_VSHIFT (I^2C-Register subaddress 6 hex, bit 7) is set.

Blank Field Mode

Software Control: I^2C-Register subaddress 7 hex, bits 0-3, (BLANK_F0 - BLANK_F3)

The Blank Field Mode allows the user to define which fields of the sequence of the 100 Hz display fields are displayed or blanked. If all the four control bits are cleared the normal active display appears. If one bit is set the corresponding display field will be blanked.

In the AABB mode a blanking of every second field generates a display which is similar to a normal 50 Hz screen. The elimination of the large area flicker can be demonstrated by switching from this mode to a normal 100 Hz display. The blank field mode is normally used for testing purposes.

Selection of the Colour Decoder Concept

Software Control: I^2C-Register subaddress 7 hex, bit 4 DCD

Normally the SAA 4977 is implemented in a concept with an analog colour decoder. In this case the acquisition clock is generated by the SAA 4977 and the internal ADC is used. If the control bit DCD (Digital

Colour decoder Concept) is set the acquisition clock has to be supplied from external. The digital data are directly fed into the first field memory. From the point of software control all horizontal acquisition register values have to be divided by the factor two. The analog frontend part of SAA 4977 V1C should be switched into the stand-by mode.

Select Field Recognition

Software Control: I^2C-Register subaddress 7 hex, bit 7 (SFR)

The field recognition that means the assignment of the video fields (even and odd) can be defined via the control bit SFR

Field length limit control

Software Control: I^2C-Register subaddress 2 hex, bit 5 (DIS_VLIMIT)

In the standard mode the deviation of the field length compared to PAL and NTSC is limited to 6 lines by the control software. If this limit shall be disabled the control bit DIS_VLIMIT has to be set.

Via enable bits the most important signals of the memory controller can be defined by the user. This allows a very flexible use of the SAA 4977 also for changed conditions in the application. Many signals are 9 bit values. If one signal is switched to a direct user control the corresponding I^2C registers for the signal start and stop values are enabled. These registers define the lower 8 bit of the complete 9 bit values. The MSBs are defined via an additional MSB register in which only those bits are processed by the software which belong to signals which are set to direct control. This means the MSB register is not activated separately.

DAC blanking control

Software Control: I^2C-Register subaddress 9 hex, bit 7 (SET_VBDA), subaddress 0A hex, bit 1 (SET_HBDA)

The bit SET_VBDA enables the direct control of the vertical blanking time for the DAC of the SAA 4977 via the I^2C registers subaddress 0B hex (VBDASTA, start value), subaddress 0C hex (VBDASTO, stop value) and subaddress 0D hex (MSB_REG1, MSB control). The MSB of the start value is controlled via bit 0 (MSB_VBDASTA) in the register MSB_REG1. The MSB of the stop value is defined via bit 1 (MSB_VBDASTO). The sensible programming range of VBDA depends on the field length of the source (PAL 0 to 138 hex, NTSC 0 to 106 hex). If the programmed values are higher than the number of lines of the source (VCR fast forward) the memory controller stops the signal automatically.

The horizontal signal part of the blanking can be controlled in the same way. The bit SET_HBDA enables the direct control of the horizontal blanking time for the DAC via the I^2C registers subaddress 10 hex (HBDASTA, start value), subaddress 11 hex (HBDASTO, stop value) and subaddress 16 hex (MSB_REG2, MSB control). The MSB of the horizontal start value is controlled via bit 2

(MSB_HBDASTA) in the register MSB_REG2. The MSB of the horizontal stop value is defined via bit 3 (MSB_HBDASTO). The programming range of HBDA is 0 to 1FF hex.

HDAV control

Software Control: I^2C-Register subaddress 0A hex, bit 0 (SET_HDAV)

If the control bit SET_HDAV is set a direct control of the horizontal data valid signal for the chroma display data is enabled. The start value is defined via I^2C register subaddress 0E hex (HDAVSTA), the corresponding MSB via I^2C register subaddress 16 hex, bit 0 (MSB_HDAVSTA). The stop value is defined via I^2C register subaddress 0F hex (HDAVSTO), the corresponding MSB via I^2C register subaddress 16 hex, bit 1 (MSB_HDAVSTO).

HRE control

Software Control: I^2C-Register subaddress 0A hex, bit 2 (SET_HRE)

If the control bit SET_HRE is set a direct control of the horizontal read enable signal fed to PROZONIC, MELZONIC or to the first field memory in the single field concept is enabled. The start value is defined via I^2C register subaddress 12 hex (HRESTA), the corresponding MSB via I^2C register subaddress 16 hex, bit 4 (MSB_HRESTA). The stop value is defined via I^2C register subaddress 13 hex (HRESTO), the corresponding MSB via I^2C register subaddress 16 hex, bit 5 (MSB_HRESTO).

HBLND control

Software Control: I^2C-Register subaddress 0A hex, bit 3 (SET_HBLND)

The control bit SET_HBLND enables the direct control of the horizontal display signal HBLND. The start value is defined via I^2C register subaddress 14 hex (HBLNDSTA), the corresponding MSB via I^2C register subaddress 16 hex, bit 6 (MSB_HBLNDSTA). The stop value is defined via I^2C register subaddress 15 hex (HBLNDSTO), the corresponding MSB via I^2C register subaddress 16 hex, bit 7 (MSB_HBLNDSTO).

CLV control

Software Control: I^2C-Register subaddress 0A hex, bit 5 (SET_CLV)

If the control bit SET_CLV is set a direct control of the clamping signal CLV is possible. This signal is fed to the ADC of the SAA 4977 internally. The start value is controlled via I^2C register subaddress 18 hex (CLVSTA). The stop value is defined via I^2C register subaddress 19 hex (CLVSTO). As the CLV signal is only programmable in steps of four acquisition clocks there is no need for an additional MSB control.

HWE control

Software Control: I^2C-Register subaddress 0A hex, bit 6 (SET_HWE)

If the control bit SET_HWE is set a direct control of the horizontal write enable signal fed to the first field memory is enabled. The start value is defined via I^2C register subaddress 1A hex (HWESTA), the corresponding MSB via I^2C register subaddress 0D hex, bit 2 (MSB_HWESTA).

The stop value is defined via I^{2}C register subaddress 1B hex (HWESTO), the corresponding MSB via I^{2}C register subaddress 0D hex, bit 3 (MSB_HWESTO).

HDDEL control

Software Control: I^{2}C-Register subaddress 0A hex, bit 4 (SET_HDDEL)

A direct control of the memory controller register HDDEL via I^{2}C register subaddress 17 hex is enabled if the control bit SET_HDDEL is set. The register HDDEL defines a fine delay of the horizontal output signals of the SAA 4977 with display clock accuracy. The delay adjustment may be necessary for changes in the concept to ensure a correct processing of the colour difference signals which are coded in a serial format (4:1:1).

Field recognition control

Software Control: I^{2}C-Register subaddress 0A hex, bit 7 (SET_FRG)

The software allows an adjustment of the field recognition in the SAA 4977 if the control bit SET_FRG is set. Normally there is no need for the user to change the corresponding settings. The SAA 4977 V1C can also run in a digital colour decoder concept in which the acquisition clock is not equal 16 MHz and even not line-locked (facq <= 32 MHz). For this configuration or sync slicers with an output timing which is very different from the TDA 2579 or TDA 9141 the following registers HRA, HVA, HP have to be redefined.

HRA control

The signal HRA is started with the H-Counter value 0 and should stop in the middle of the line. This results in a default value of 80 Hex for the stop of HRA in the 16 MHz application. For changed acquisition frequencies the value has to be adapted. The input frequency is predivided by the factor four in a digital colour decoder concept. The setting of HRA_STO is controlled via I^{2}C register subaddress 1C hex.

HVA control

The registers HVA_1 and HVA_2 (I^{2}C register subaddress 1D and 1E hex) define two pulses which sample the vertical synchronization pulse Vacq. The programming of these pulses should be done in a way that the distance of the rising Vsync edge and the HVA_1 and HVA_2 pulses equals about 16 µs. The distance from HVA_1 to HVA_2 has to equal 32 µs.

HP control

The user can change the setting of the SAA 4977 V1C register for the position of the pulse HP1. This pulse has to be programmed around 32 µs shifted to HVA_1 to ensure a stable picture in case of unstable sources (VCR trick modes). There are four pulses HP1 to HP4 with a frequency of 4 x fh and a distance of 16 µs which are used for incrementing the vertical display counter. Only HP1 is directly programmable via I^{2}C register subaddress 2B hex. The values for the other three pulses are calculated automatically by the software. The distance is 40 Hex.

4.3.2 MELZONIC/PROZONIC control

Noise reduction

Software Control: I^{2}C-Register, subaddress 4 hex, bit 0 and 1 (NR0, NR1)

The recursive noise reduction can be set to three levels (low, medium, high). For investigation purposes a direct control of the PROZONIC/MELZONIC noise reduction registers is possible. The direct control activated by the bit SET_NR (I^{2}C-Register, subaddress 9, bit 2) includes the definition of the K-curve and the setting of the filter coefficients (I^{2}C-Registers subaddress 1F to 25 hex). Via the control bit NR_INT (I^{2}C register, subaddress 4 hex, bit 6) the noise reduction is cancelled each second for the duration of one single display field.

Split Screen

Software Control: I^{2}C-Register subaddress 4 hex, Bits 2,3 (SPS0, SPS1)

The screen can be split into two halves by the Split Screen feature. One half is showing a noise reduced picture the other the performance of the original source. The splitting can be done in horizontal or vertical direction. The mode allows a direct comparison of the original and noise reduced picture on the screen.

Selection of the Application Concept

Software Control: I^{2}C-Register subaddress 7 hex, bits 5 and 6 (CON0 and CON1)

Via the control bits CON0 and CON1 the hardware concept can be chosen. Both bits cleared switch to the single field concept. CON0 set and CON1 cleared choose the PROZONIC concept. If CON1 is set the MELZONIC concept is selected.

FILL control

Software Control: I^{2}C-Register subaddress 9 hex, bit 3 (FILL)

The SAA 4977 V1C concept allows two different ways to obtain a fill colour covering the whole screen as background for a display on screen area. The first possibility is to activate the SAA 4977 V1C control bit FILL_MEM (I^{2}C-REG. subaddress 35 hex, bit 5). In this case the ADC data output bus is fixed and a blue screen will appear.

The control bit FILL can only be used in the MELZONIC concept and uses the fill option of the SAA 4991. If FILL is set a direct access to the MELZONIC registers FIXCOL_Y and FIXCOL_UV is enabled via the I^{2}C-Registers subaddress 27 and 28 hex.

Direct control of the Natural Motion Parameters

Software Control: I^{2}C-Register subaddress 9 hex, bit 0 (NM_CTL)

If the control bit NM_CTL is set the two I^{2}C registers BAD_LIMIT and RELIABILITY_THRESHOLD are activated and allow the user to change the behaviour of the natural motion processing.

BAD_LIMIT

Software Control: I^{2}C-Register subaddress 29 hex, BAD_LIMIT

The software switches back to a simple LFR mode if the Melzonic read register NR_BAD_RANGES delivers values larger than BAD_LIMIT. This threshold can be controlled by the user via I^{2}C bus. The MELZONIC read register value NR_BAD_RANGES is the sum of bad ranges per field. A bad range is a range in which at least “NR_BADBLOCKS” blocks have an SAD above the threshold (reliability). The MELZONIC value NR_BADBLOCKS (bits 4,5,6 in register nrbadblocks_nr_lines_53) defines the number of neighbouring bad blocks in a range until which a range is marked as “bad”.

Reliability Threshold

Software Control: I^{2}C-Register subaddress 2A hex, RELIABILITY_THRESHOLD

Via the I^{2}C register 2A a threshold for the maximum prediction error (SAD within a block) can be defined if the bit NM_CTL is set. The MELZONIC read register value NR_BAD_RANGES is effected by this setting and corresponding the fallback behaviour of the natural motion.

Direct control of HOR_DEL register

Software Control: I^{2}C-Register subaddress 09 hex, bit 1 (SET_ HOR_DEL)

If the control bit SET_HOR_DEL is set a direct control of the MELZONIC register HOR_DELAY is enabled (see MELZONIC data sheet) via the I^{2}C register subaddress 26 hex. This register allows a fine delay of the MELZONIC memory control output signals. with clock accuracy. It further more allows an adjustment of the chroma reformatting for a correct internal chroma processing.

Vector Overlay

Software Control: I^{2}C-Register subaddress 9 hex, bit 5 (VEC_OVL)

For testing purposes the MELZONIC control bit VECTOR_OVERLAY can be set via the I^{2}C control bit VEC_OVL. In this case the estimated vectors are displayed as a coloured overlay. The shade of the colour is correlated to the direction of movement. The saturation is dependent on the speed of movement.

4.3.3 Port Pin Control

Software Control: I^2C-Register subaddress 8 hex, bit 0 - bit 4

The free port pins of the µ-Controller core in the SAA 4977 can be controlled via I^2C bus. The polarity of the port pins is switched synchronized to VDFL this means synchronized to the display. The port pins P1.1 to P1.5 can be controlled.

4.3.4 Limeric control

Software Control: I^2C-Register subaddress 2C hex to 2E hex

The LIMERIC (SAA 4945) allows a line-based noise reduction for the single field memory concept. The bits L_NR0 to L_NR 2 (subaddress 2C, bit 0 to 2) define the amount of noise reduction. The control bit DEM (bit 3) supports a demonstration mode in which the picture is vertically split into a noise reduced and original area. Via the bit WES (bit 4) the WE signal can be shifted by one clock. The control bit EX_THR (bit 5) enables an external control of the noise reduction threshold via I^2C register subaddress 2D hex. The register WVAL (subaddress 2E, wanted value) defines a threshold for the sensitivity of the noise detection.

4.3.5 Datapath control

Horizontal Compression

Software Control I^2C Register subaddress 1 hex, bit 4 and 5 COMP0 and COMP1, bit 6 and bit 7 (PP0 and PP1)

The SAA 4977 supports two different compression modes for 14:9 and 16:9 display modes (1.17 and 1.33). These modes can be activated via the control bits COMP0 and COMP1. These bits change the timing of the memory control signals. Additionally the data compressor of the SAA 4977 is activated automatically via the datapath register. Three different horizontal positions (left, middle and right) are provided by the software. If the user wants to use different picture positions of the display they can be obtained by a direct I^2C control of the horizontal display control signals (HRE, HBDA and side panels).

Screen fade

Software Control: I^2C-Register subaddress 4 hex, Bit 4,5 (SCF0, SCF1)

The screen fade feature can be used to “fade out” a picture like closing curtains. This is done by the control SW by continuously changing the setting of the side panel start and stop values of SAA 4977 until a homogenous coloured picture is visible. The function is also available the other way round where the picture is “faded in”. The colour difference and luminance values of the faded area are defined by the datapath registers for the side panels (SIDEP_OVL_UV and SIDEP_OVL_Y). As

long as the screen fade processing has not finished the bit SCREEN_FADE_ACTIVE in the status byte is set. Additionally the progress of the screen fade operation can be traced in the SCREEN_FADE_COUNT read register. The read value starts with 0 if the screen fade processing just starts. The value is incremented during the fade procedure until the final position is reached. If the fade processing has finished the read register contains the value FF hex.

Side panel control

Software Control: I^2C-Register subaddress 09 hex, bit 4 (SET_SIDEP)

The side panels needed for the compress modes on a 16:9 display are automatically controlled fitting to the chosen compress mode (see 3.2.2). If the control bit SET_SIDEP is set the side panels are controlled by the user via the I^2C registers subaddress 3D hex (LEFT_SIDEPANEL) and 3E hex (RIGHT_SIDEPANEL). The luminance and chroma values are controlled via I^2C registers subaddress 3B hex (SIDEP_OVL_UV) and 3C hex (SIDEP_OVL_Y).

4.4 Datapath translator registers

Software Control: I^2C-Register subaddress 30 - 3F hex

Via the I^2C registers with subaddress 30 to 3F hex the SAA 4977 datapath registers can be directly accessed. The datapath registers are initialized after power-on but not changed by any other routines than the I^2C bus.

Exceptions:

The sidepanel values are switched to adapted sensible values if a compress mode has been activated. These values can be overruled with an I^2C bus transmission to the sidepanel I^2C registers.

The datapath compression bits are not under direct I^2C control. They are activated in combination with the compression control bits COMP0 and COMP1

VRES_DIS is set automatically if the Progressive Scan mode is activated. The vertical timing of the display is delayed towards the acquisition in this mode. Therefore the internal reset for the vertical display counters has to be disabled

For a detailed functional description of the datapath please refer to the application notes AN97057 and AN97071.

4.5 SNERT interface

Via the SNERT interface all register data for PROZONIC, MELZONIC or LIMERIC dependant on the chosen hardware configuration is transmitted. The internal SNERT pins of the µC Core of the SAA4977 are directly connected to the pins of the SAA4977 V1C.